1. (Amended) An input protection circuit according to claim 21, wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, and said fourth well region and the base of the second lateral bipolar transistor are connected to said reference potential node.

3. (Amended) An input protection circuit according to claim 21, wherein said input terminal is connected to said third well region, said fourth well region and the base of said second lateral bipolar transistor are connected to said first impurity doped region, and said second impurity doped region and the base of the first lateral bipolar transistor are connected to said reference potential node.

4. (Amended) An input protection circuit according to claim 3, further comprising a current limiting resistor formed on an insulating layer formed in the principal surface area of said semiconductor substrate, wherein said input terminal is connected via said current limiting resistor to said third well region.

5. (Amended) An input protection circuit, according to claim 22, wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, and said third well region and the base of the second lateral bipolar transistor are connected to said reference potential node.

7. (Amended) An input protection circuit, according to claim 22, wherein said input terminal is connected to said second well region, said

third well region and the base of said second lateral bipolar transistor are connected to said first impurity doped region, and said second impurity doped region and the base of the first lateral bipolar transistor are connected to said reference potential node.

21. (New) An input protection circuit comprising:

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate;

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate,

an input terminal formed on said semiconductor substrate;

a circuit formed in said semiconductor substrate, and connected to said input terminal; and

a reference potential node formed on said semiconductor substrate;

wherein said first and second lateral bipolar transistors are connected in

series between said input terminal and said reference potential node.

22. (New) An input protection circuit comprising:

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

second and third well regions of the second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

an input terminal formed on said semiconductor substrate;

a circuit formed on said semiconductor substrate, and connected to said input terminal; and

a reference potential node formed on said semiconductor substrate;

wherein said first and second lateral bipolar transistors are connected in series between said input terminal and said reference potential node.